UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/390,079	09/03/1999	DARREN KERR	112025-0167	6305

7590 01/22/2002

CHARLES J BARBAS
CESARI AND MCKENNA
30 ROWES WHARF
BOSTON, MA 02110

EXAMINER
ELLIS, RICHARD L

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

HG

Office Action Summary

Application No.	Applicant(s)	
09/390,079	Kerr et al.	
Examiner	Group Art Unit	
Richard Ellis	2183	

--The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address--

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (Three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) Months from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☐ Responsive to communication(s) filed on _____.

☐ This action is FINAL

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-21. is/are pending in the application.

☐ Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-21. is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119(a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 3.

☒ Notice of References Cited, PTO-892

☒ Notice of Draftsperson's Patent drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

1. Claims 1-21 are presented for examination.

2. Applicant's information disclosure statement of May 25, 2001, paper number 3, could not be completely considered because although applicant did provide copies of the patent specifications for the cited patent references, those copies are identified only by attorney docket numbers, whereas the form 1449 identifies the application by US patent application serial number. As there is no easy way to ascertain which attorney docket number on the copies corresponds to which US patent application serial number, it is impossible to know if the supplied copies are indeed the intended copies for consideration. In responding to this office action applicant should provide a table indicating the correspondence between the attorney docket numbers on the supplies copies and the US patent application serial numbers used on the form 1449. If applicant supplies this correspondence table, then the supplied information will be considered.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

4. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1-21 are rejected under 35 USC 102(e) as being clearly anticipated by Asato, U.S. Patent 6,145,074.

Asato taught (e.g. see figs. 1-17) the invention as claimed (as per claim 1), including a data processing ("DP") system comprising:

A) apparatus for enabling an instruction (figs. 1 and 5) to control data flow bypassing hardware (col. 2 lines 53-58) within a processor of a programmable processing engine (figs. 2, 4, 6), the apparatus comprising;

B) a pipeline of the processor (fig. 2. element 2, fig. 4, element 2, fig. 6, elements 21-1 to 21-4, col. 5 line 28, col. 6 lines 17-18 and 50-53), the pipeline having a plurality of stages including instruction decode, writeback and execution stages (col. 1 lines 26-31,

col. 7 lines 38-65), the execution stage having a plurality of parallel execution units (fig. 6), and;

C) an instruction set of the processor (figs. 1 and 5), the instruction set defining a register decode value (b1, b2, p1, p2) that specifies one of source operand bypassing and result bypassing from a previous instruction executing in pipeline stages of the processor (col. 5 lines 14-24 and col. 6 lines 36-43).

6. As to claim 2, Asato taught a register file (fig. 2, 1, fig. 4, 1, fig. 6, 21-1 to 21-4) containing a plurality of general purpose registers for storing intermediate result data processed by the execution units (col. 5 lines 28 and 45-48), and;

a memory (inherently present as a main memory for the computer) for storing one of transient data unique to a specific process (an inherent use of a computers main memory) and pointers referencing data structures (also an inherent use of a computers main memory).

7. As to claim 3, Asato taught that the register decode value comprises one of a result bypass (RRB) operand (fig. 2, b1, bp2) and an inner-unit result bypass (RIRB) operand (b2, bp1), each of which explicitly controls data flow within the pipeline of the processor (col. 2 lines 53-57, col. 5 lines 45-67).

8. As to claim 4, Asato taught that the execution units comprised a current execution unit (fig. 6, 21-1) and an alternate execution unit (21-2), and wherein the RRB operand denotes the current execution unit and the RIRB operand denotes the alternate execution unit (col. 6 line 44 to col. 7 line 9).

9. As to claim 5, Asato taught that the RRB operand (fig. 2, b1) explicitly infers feedback of the data delivered from a current one of the execution units (2) to an input register of the current execution unit (3) over a feedback path (bp1, bp2).

10. As to claim 6, Asato taught that the writeback stage comprises an interstage register (fig. 2, 3, 4) and wherein the RRB operand (7, 8) enables bypassing write-back of the data processed by the execution units (10, 13) to one of the register file (1) or the interstage register of the writeback stage (bp2).

11. As to claim 7, Asato taught that the register decode value comprises a source bypass

(RISB) operand that allows source operand data to be shared among the parallel execution units of the pipelined processor (fig. 6, col. 6 line 44 to col. 7 line 12).

12. As to claim 8, Asato taught that the execution units comprise a main execution unit (fig. 6, 21-1) and a secondary execution unit (21-2), and wherein the RISB operand allows the secondary execution unit to receive data stored at an effective memory address specified by a displacement operand in the previous instruction executed by the main execution unit (col. 6 line 44 to col. 7 line 12).

13. As to claims 9-21, they do not teach or define above the invention claimed in claims 1-8 and are therefore rejected under Asato for the same reasons set fourth in the rejection of claims 1-8, supra.

14. As to claims 13 and 14, Asato taught that his system was intended for obviating the need for additional hardware, including scoreboard addressing areas or data structures (col. 2 lines 48-65).

15. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

16. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone numbers for this Group are: After-final: (703) 746-7238; Official: (703) 746-7239; Non-Official/Draft: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
Primary Examiner
Art Unit 2183

Richard Ellis
January 17, 2002